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METHOD AND APPARATUS FOR LOW COST SIGNATURE
TESTING FOR ANALOG AND RF CIRCUITS

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TC 2800 MAIL ROOM

5 This application is a continuation-in-part of the inventors' prior application
Serial No. 09/575,488, filed May 19, 2000, entitled Method for Testing Circuits, and
claims the benefit of the provisional application Serial No. 60/197,749, filed April 18,
2000, entitled ATPG for Prediction of Analog Specifications, and Serial No.
60/203,602, filed May 12, 2000, entitled Test Generation for High Frequency and RF
10 Circuits, each incorporated by reference in their entireties herein.

Background of the Invention

The present invention relates to a method and apparatus for low cost signature
testing for testing analog and RF circuits. More particularly, the invention relates to
15 such a method and apparatus for use in manufacturing testing, and for use in
monitoring the manufacturing process.

Analog and RF circuits are characterized by a set of performance parameters
that typically vary continuously over a range. These performance parameters result
from design as modified by variations in the manufacturing process that occur over
20 time. Because of this variation, it is often necessary to test at least some of the
circuits produced by a given manufacturing process to ensure that the performance
parameters of the circuits fall within given specification limits.

However, traditional testing methods impose an increasing burden in the form
of test time as a result of the ever increasing complexity and speeds of analog and RF
25 circuits. For example, straightforward testing employs automated or automatic test
equipment ("ATE") to stimulate the circuit under test (CUT) in a manner designed to
induce the circuit to provide an output which directly reflects the value of each
performance parameter which it is desired to test. The output is used to determine
whether the parameter is within specification limits, in which case the CUT is
30 considered "good" or is considered to "pass," or whether the parameter is outside the
specification limits, wherein the CUT is considered "bad" or is considered to "fail."